In the claims:

Please cancel claims 31-33.

Please amend claims 1, 10, 14, 19, 23, and 27 as follows:

1.   (Currently Amended) A computer system,

comprising:

a non-cached multi-ported memory;

a main memory;

a central processing unit coupled to the multi-ported

memory;

a bus configured to communicate with one or more peripheral

devices, the bus coupled to the multi-ported memory and

configured to access the multi-ported memory independently of

the central processing unit;

wherein the computer system is configured so that control

accesses from the central processing unit are directed to the

multi-ported memory and not to the main memory and data accesses

from the central processing unit are directed to the main memory

and not to the dual-ported memory.

2.   (Original) The system of claim 1, further comprising

an operating system executing on the central processing unit,

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wherein the operating system is configured such that accesses to the multi-ported memory are not cached.

3. (Original) The system of claim 1, wherein the multi-ported memory is dual-ported.

4. (Original) The system of claim 1, wherein the multi-ported memory is embedded within a memory controller.

5. (Original) The system of claim 4, wherein the multi-ported memory and memory controller are integrated into a single chip.

6. (Previously Amended) The system of claim 1, wherein the multi-ported memory is chosen from the group consisting of static random access memory and dynamic random access memory.

7. (Original) The system of claim 1, wherein the multi-ported memory stores reservation bits mapped to blocks of general-purpose memory in the multi-ported memory.

8.   (Original) The system of claim 1, wherein virtual addresses within multi-ported memory are mapped to physical addresses with smart addressing.

9.   (Original) The system of claim 1, wherein the coupling of the peripheral device to the memory controller includes an input/output bus.

10.   (Currently Amended) A method comprising:

routing a data access from a peripheral device to a first memory in the computer and not to a second memory in the computer; and

routing a status access from a peripheral device to [a] the second memory in the computer and not to the first memory in the computer.

11.   (Original) The method of claim 10, wherein the first memory comprises main memory.

12.   (Original) The method of claim 10, wherein the second memory comprises memory included in a memory controller.

13. (Original) The method of claim 10, wherein the second memory is dual-ported.

14. (Currently Amended) An article comprising a computer-readable medium which stores computer-executable instructions for memory accessing, the instructions causing a machine to:

route a data access from a peripheral device to a first memory in the computer and not to a second memory in the computer; and

route a status access from the peripheral device to [a] the second memory in the computer and not to the first memory.

15. (Original) The article of claim 14, wherein the computer includes an input/output controller.

16. (Original) The article of claim 14, wherein the first memory comprises main memory.

17. (Original) The article of claim 14, wherein the second memory comprises memory included in a memory controller.

18. (Previously Amended) The article of claim 14, wherein the second memory is dual-ported.

19. (Currently Amended) A method comprising:

routing the a data access from a central processing unit to a first memory in the computer <u>and not to a second memory in the computer</u>; and

routing a control access from the central processing unit to [a] <u>the</u> second memory in the computer <u>and not to the first memory</u>.

20. (Original) The method of claim 19, wherein the first memory comprises main memory.

21. (Previously Amended) The method of claim 19, wherein the second memory is included in a memory controller.

22. (Original) The method of claim 19, wherein the second memory is dual-ported.

23. (Currently Amended) An article comprising a computer-readable medium which stores computer-executable instructions for memory accessing, the instructions causing a machine to:

route a data access from a central processing unit to a

first memory in the computer and not to a second memory in the

computer; and

route a control access from the central processing unit to

[a] the second memory in the computer and not to the first

memory in the computer.

24.   (Original)   The article of claim 23, wherein the first

memory comprises main memory.

25.   (Original)   The article of claim 23, wherein the

second memory comprises memory included in a memory controller.

26.   (Original)   The article of claim 23, wherein the

second memory is dual-ported.

27.   (Currently Amended)   An integrated circuit comprising:

a memory controller configured to communicate with a CPU, a

peripheral device, and a main memory, the memory controller

including a multi-ported memory, wherein the memory controller

is to direct control accesses for the CPU [are directed] to the

multi-ported memory and not to the main memory, and wherein the

<u>memory controller is to direct</u> data accesses for the CPU [are

directed] to the main memory <u>and not to the multi-ported memory</u>.

28. (Original) The integrated circuit of claim 27,

wherein the multi-ported memory is dual-ported.

29. (Previously Amended) The integrated circuit of claim

27, wherein the multi-ported memory is chosen from the group

consisting of static random access memory and dynamic random

access memory.

30. (Original) The integrated circuit of claim 27,

wherein the multi-ported memory stores reservation bits mapped

to blocks of general-purpose memory in the multi-ported memory.

31. (Cancelled)

32. (Cancelled

33. (Cancelled)